TLA5000 Series Logic Analyzers

▶ TLA5201 • TLA5202 • TLA5203 • TLA5204

▶ Features & Benefits

500 ps (2 GHz)/32 Mb Deep Memory Timing to Capture Intermittent Events over a Wide Time Window

125 ps Resolution MagniVu™ Timing Simultaneous with State or Deep Memory Timing Acquisition to Find Elusive Timing Problems Quickly, Without Double Probing

Glitch and Setup/Hold Violation Triggering and Display to Find and Display Elusive Hardware Problems

235 MHz State Acquisition Provides Analysis of High-speed Synchronous Digital Circuits

iView™ Time-correlated Digital-analog View to Clearly See How Analog Anomalies are Affecting Your Digital Signals

34/68/102/136 Channel Configurations Offer Flexible Solutions to Fit any Budget

▶ Applications

Digital Hardware Verification and Debug

Monitoring and Measurement of Digital Hardware Performance

Single Microprocessor or Bus Debug

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TLA5000 Series Logic Analyzers Combine Debug Power with Simplicity and Affordability

The affordable TLA5000 Series logic analyzers make high-speed timing resolution, fast state acquisition, deep memory, and sophisticated triggering available to any digital designer who needs to identify initialization failures, operation crashes and intermittent operation. For first-time as well as experienced logic analyzer users, the TLA5000 Series is ideal for single-bus timing and state analysis. An intuitive user interface, familiar Windows-based desktop and OpenChoice™ networking and analysis features make the TLA5000 Series logic analyzers easy to network into your design environment.

500 ps timing resolution and 32 Mb memory depth with simultaneous 125 ps MagniVu™ timing resolution within each acquisition means you can measure digital signal timing on increasingly faster signals with confidence. With MagniVu timing resolution, find difficult problems such as digital logic errors, glitches, setup/hold violations, and crosstalk quickly. Use setup/hold violation triggering and display to validate setup/hold performance of digital devices.

Today, most designs can have both digital and analog anomalies. With iView™ time-correlated digital-analog view, you'll clearly see how analog anomalies are affecting your digital signals – right on your logic analyzer display.

Tektronix
Enabling Innovation

▶ Characteristics

General

Number of Channels –
(all channels are acquired including clocks).
TLA5201: 34 channels (2 are clock channels).
TLA5202: 68 channels (4 are clock channels).
TLA5203: 102 channels (4 are clock and 2 are qualifier channels).
TLA5204: 136 channels (4 are clock and 4 are qualifier channels).

Time Stamp – 51-Bits at 125 ps resolution (3.25 days duration).

Clocking/Acquisition Modes – Internal, internal 2X, internal 4X, external 2X, source synchronous. 125 ps (8 GHz) MagniVu™ high-speed timing is available simultaneous with all modes.

Input Characteristics (with P6417, P6418, P6419 or P6434 probes)

Capacitive Loading –
<0.7 pF typical data/clock (P6419).
1.4 pF typical data; 2 pF typical clock (P6418).
2 pF typical data/clock (P6417, P6434).

Threshold Selection Range – From –2.0 V to +4.5 V in 5 mV increments.
Threshold presets include TTL (1.5 V), CMOS (1.65 V), ECL (–1.3 V), PECL (3.7 V), LVPECL (2.0 V), LVCMOS 1.5 V (0.75 V), LVCMOS 1.8 V (0.9 V), LVCMOS 2.5 V (1.25 V), LVCMOS 3.3 V (1.65 V), LVDS (0 V), and user-defined.

Threshold Selection Channel Granularity – Separate selection for each of the clock/qualifier channels and one per group of 16 data channels.

Threshold Accuracy (including probe) – ±(100mV).

Input Voltage Range –
Operating: –2.5 V to 5.0 V.
Nondestructive: ±15 V.

Minimum Input Signal Swing –
±250mV (P6417, P6418, P6419).
±300mV (P6434).

Input Signal Minimum Slew Rate – 200 mV/ns typical.

State Acquisition Characteristics (with P6417, P6418, P6419 or P6434 probes)

Maximum State Clock Rate – 235 MHz.

Maximum State Data Rate – 470 Mb/s.

State Memory Depth with Timestamps (half/full channels) – 1 Mb/512 Kb, 4/2 Mb, 16/8 Mb.

Setup and Hold Time Selection Range – 16 ns range that may be shifted towards the setup region by 0 ns [+8, –8] ns, 4 ns [+12, –4] ns, or 8 ns [+16, 0] ns.

Setup-and-Hold Window – All Channels: 1.5 ns typical.

Minimum Clock Pulse Width –
1.5 ns (P6434).
1.25 ns (P6417, P6418, P6419).

Demux Channel Selection – Channels can be demultiplexed to other channels through user interface with 8 channel granularity

Timing Acquisition Characteristics (with P6417, P6418, P6419 or P6434 probes)

MagniVu™ Timing –
125 ps (8 GHz).
Storage rate adjustable to 250 ps, 500 ps, 1 ns, and 2 ns.

MagniVu Timing Memory Depth – 16 Kb per channel, with adjustable trigger position.

Deep Memory Timing Resolution (quarter/half/full channels) – 500 ps/1 ns/2 ns to 50 ms.

Deep Memory Timing Memory Depth (quarter/half/full channels with timestamps and with or without transitional storage) –
2 Mb/1 Mb/512 Kb, 8/4/2 Mb, 32/16/8 Mb per channel.

Deep Memory Timing Memory Depth with Glitch Storage Enabled – Half of default main memory depth.

Channel-to-Channel Skew – 1 ns.
900 ps typical.

Minimum Recognizable Pulse/Glitch Width (single channel) – 1 ns (P6417, P6418, P6419)
1.25 ns (P6434).

Minimum Detectable Setup/Hold Violation – 250 ps.

Minimum Recognizable Multi-channel Trigger Event – Sample period + channel-to-channel skew.

Trigger Characteristics

Independent Trigger States – 16.

Maximum Independent If/then Clauses per State – 16.

Maximum Number of Events per If/then Clause – 8.

Maximum Number of Actions per If/then Clause – 8.

Maximum Number of Trigger Events – 18
(2 counter/timers plus any 16 other resources).

Number of Word Recognizers – 16.

Number of Transition Recognizers – 16.

Number of Range Recognizers – 4.

Number of Counter/Timers – 2.

Trigger Event Types – Word, group, channel, transition, range, anything, counter value, timer value, signal, glitch, setup-and-hold violation, snapshot.

Trigger Action Types – Trigger main, trigger MagniVu™, store, don't store, start store, stop store, increment counter, decrement counter, reset counter, start timer, stop timer, reset timer, snapshot current sample, goto state, set/clear signal, do nothing.

Trigger Sequence Rate – DC to 500 MHz (2 ns).

Counter/Timer Range – 51 Bits each (>50 days at 2 ns).

Counter Rate – DC to 500 MHz (2 ns).

Timer Clock Rate – 500 MHz (2 ns).

Counter/Timer Latency – 2 ns.

Range Recognizers – Double bounded (can be as wide as any group, must be grouped according to specified order of significance).

Setup-and-Hold Violation Recognizer Setup Time Range – From 8 ns before to 7.5 ns after clock edge in 125 ps increments.

Setup-and-Hold Violation Recognizer Hold Time Range – From 7.5 ns before to 8 ns after clock edge in 125 ps increments.

Trigger Position – Any data sample.

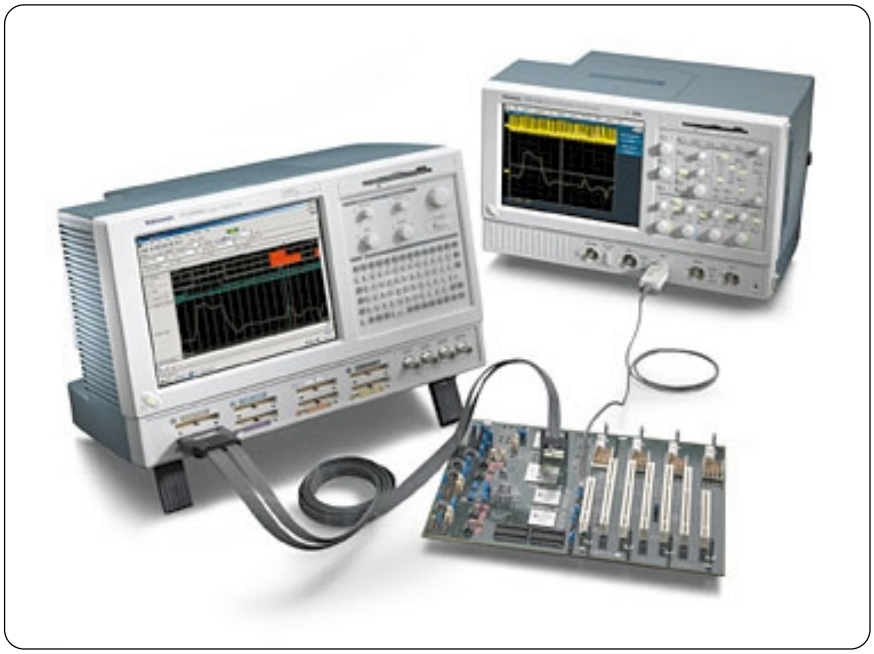
MagniVu™ Trigger Position – MagniVu position can be set from 0% to 60% centered around the MagniVu trigger.

Storage Control (data qualification) – Global (conditional), by state (start/stop), block, by trigger action, or transitional. Force main prefill selection available.

iView™ (Integrated View) Capability

TDS Oscilloscope Configuration Requirements – The iView cable does not connect fully to the TDS1000/2000 Series oscilloscopes without a GPIB extender. Tektronix recommends a standard GPIB cable as an extender, or order a cable adapter (Tektronix part number 103-0371-00). TDS2CMA Communications Extension Module required for iView capability on any TDS1000/2000 Series. TDS3GM GPIB/RS232 Interface Module required for iView capability on any TDS3000 Series. TDS3GV GPIB/RS232/VGA Interface Module required for iView capability on any TDS3000B Series. If using iView with a TDS6404, TDS6604, TDS7154, TDS7404, CSA7154, or CSA7404 order a TCA-BNC connector to be compatible with BNC cable run from a TLA7Axx module.

Number of TDS Oscilloscopes that Can Be Connected to a TLA System – 1.



▶ *TLA5000 Series with TDS5000 Series Oscilloscope.*

External Oscilloscopes Supported –
TDS1002, TDS1012, TDS2002, TDS2012, TDS2014, TDS2022, TDS2024.
TDS3012, TDS3014, TDS3032, TDS3034, TDS3052, TDS3054.
TDS3012B, TDS3014B, TDS3032B, TDS3034B, TDS3052B, TDS3054B.
TDS5032, TDS5034, TDS5052, TDS5054, TDS5104.
TDS6404, TDS6604.
TDS7054, TDS7104, TDS7154, TDS7404.
TDS684C, TDS694C.
CSA7154, CSA7404.
TDS754C, TDS784C, TDS724D, TDS754D, TDS784D, TDS794D.

TLA Connections – USB, Trigger In, Trigger Out, Clock Out.

TDS Connections – GPIB, Trigger In, Trigger Out, Clock In (when available).

Setup – iView external oscilloscope wizard automates setup.

Data Correlation – After TDS oscilloscope acquisition is complete, data is automatically transferred to the TLA and time correlated with the TLA acquisition data.

Deskew – TDS and TLA data is automatically deskewed and time correlated when using the iView external oscilloscope cable.
iView External Oscilloscope Cable Length – 2 m.

TLA5000 Series Logic Analyzers

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PC Characteristics

Operating System – Microsoft Windows 2000 Professional SP3.

Processor – Intel Celeron 2.0 GHz.

Chipset – Intel 845GV.

DRAM – 512 MB SDRAM.

Sound – 16-Bit I/O and Mic In port.

Hard Disk Drive – 80 GB.

CD-ROM – Internal 24/10/24 CD-RW.

Floppy Disk Drive – Built-in 3.5 in. 1.44 MB drive.

Integral Controls

Front-panel Display –
Size: 10.4 in. diagonal.
Type: Active-matrix color TFT LCD with backlight.
Resolution: 1024x768.
Colors: 256 K.

Simultaneous Display Capability – The front-panel and secondary displays can be operated simultaneously using the same resolution. The secondary external display can be used simultaneously using an independent resolution.

Front-panel Controls – Special function knobs for instrument control and mini-QWERTY keypad.

External Peripheral Interfaces

External Display Port Type – Female DB15 SVGA connector.

External Display Resolution – Up to 1600x1200 non-interlaced at 16.8 M colors.

LAN Port Type – 10/100Base-T, RJ-45.

External Keyboard Port Type – PS2 mini-DIN.

External Mouse Port Type – PS2 mini-DIN.

Parallel Interface Port Type – Female DB25.

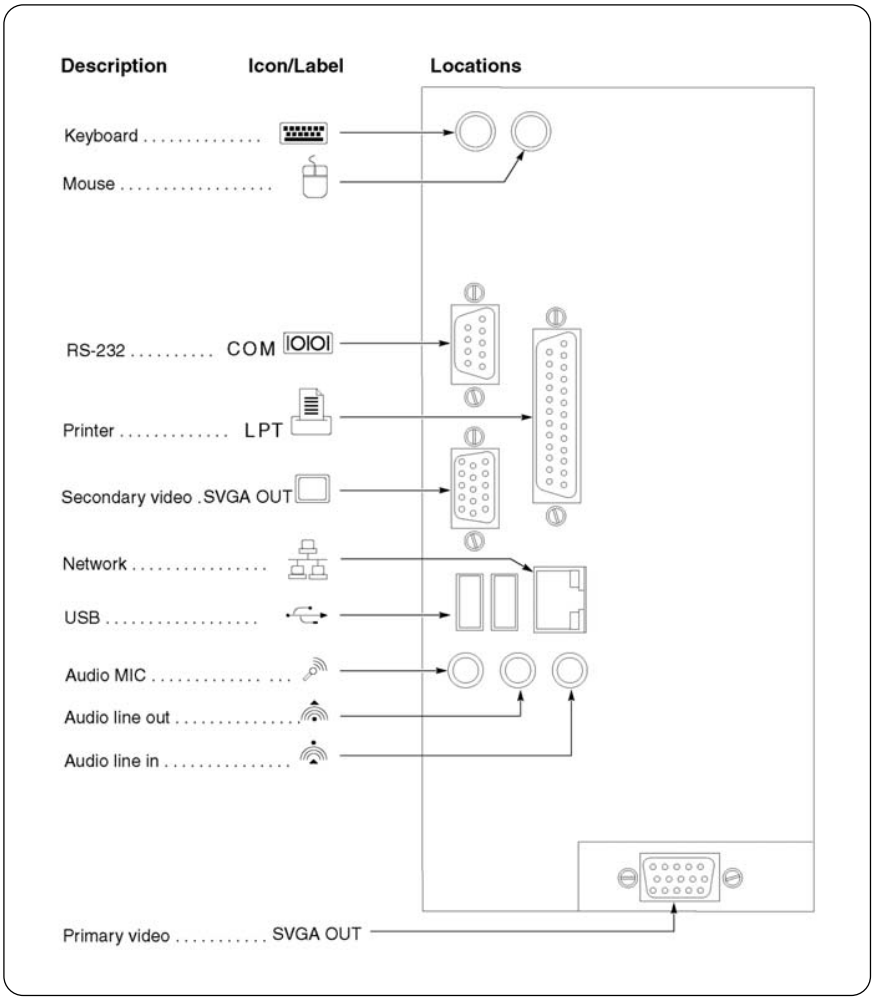
Parallel Interface Modes – Centronics mode, EPP (Extended Parallel Port), ECP (Microsoft high-speed mode).

Serial Interface Port Type – Male DB9.

Audio Out Port Type – Stereo minijack.

Mic In Port Type – Minijack.

USB Port – Two USB 2.0.



▶ *TLA5000 Logic Analyzer I/O.*

Symbolic Support

Number of Symbols/Ranges – Unlimited (limited only by amount of virtual memory available on TLA).

Object File Formats Supported

- IEEE695
- OMF 51, OMF 86, OMF 166, OMF 286, OMF 386
- COFF
- Elf/Dwarf 1 and 2
- Elf/Stabs
- TSF (if your software development tools do not generate output in one of the above formats, TSF or the Tektronix symbol file, a generic ASCII file format is supported. The generic ASCII file format is documented in the TLA User Manual). If a format is not listed, please contact your local Tektronix representative.

External Instrumentation Interfaces

System Trigger Output – Asserted whenever a system trigger occurs (TTL-compatible output, back-terminated into 50 Ω). BNC type connector.

System Trigger Input – Forces a system trigger (triggers all modules) when asserted (TTL-compatible, edge-sensitive, falling-edge latched). BNC type connector.

External Signal Output – Can be used to drive external circuitry from a module's trigger mechanism (TTL-compatible output, back-terminated into 50 Ω). BNC type connector.

External Signal Input – Can be used to provide an external signal to arm or trigger any or all modules (TTL-compatible, level-sensitive). BNC type connector.

Power

Voltage Range/Frequency – 90 to 240 VAC at 47 to 63 Hz.

Input Current – 5 A maximum at 90 VAC.

Power Consumption – 300 W maximum.

Physical Characteristics

TLA5000

Dimensions	**mm**	**in.**
Height	285	11.2
Width	438	17.5
Depth	288	11.35
Weight	**kg**	**lb.**
Net (w/o probes)	12	26
Shipping (typical)	18.5	41

Environmental

Temperature –
Operating: +5 ºC to +50 ºC.
Nonoperating: –20 ºC to +60 ºC.

Humidity –
20% to 80%.
Operating: 20% to 80% relative humidity (29 ºC maximum wet bulb temperature).
Nonoperating: 8% to 80% (29 ºC maximum wet bulb temperature).

Altitude – Operating: –1,000 ft. to 10,000 ft. (–305 meters to 3,050 meters).

Safety – UL3111-1, CSA1010.1, EN61010-1, IEC61010-1.

▶ Ordering Information

TLA5201

34 Channel, 2 GHz Deep Memory Timing with 125 ps MagniVu™ Acquisition, 235 MHz State, 512 Kb Logic Analyzer.

TLA5202

68 Channel, 2 GHz Deep Memory Timing with 125 ps MagniVu Acquisition, 235 MHz State, 512 Kb Logic Analyzer.

TLA5203

102 Channel, 2 GHz Deep Memory Timing with 125 ps MagniVu Acquisition, 235 MHz State, 512 Kb Logic Analyzer.

TLA5204

136 Channel, 2 GHz Deep Memory Timing with 125 ps MagniVu Acquisition, 235 MHz State, 512 Kb Logic Analyzer.

All Include: Mini Keyboard (119-6906-00), Optical Wheel Mouse (119-6900-00), Front Panel Cover (200-4651-00), Probe Retainer Bracket (407-4435-01), Accessory Pouch (016-1935-00), Mouse Pad (016-1524-04), TLA5000 Series Product Software CD (063-3487-02), TLA5000 Series Operating System Restore CD (063-3672-00), TLA Documentation CD (063-3671-00), TLA5000 Quick Installation Reference (071-1302-00), TLA V4.3 User Manual (071-0863-03), TLA5000 Installation Manual (071-1301-00), Certificate of Traceable Calibration, Power Cord.

Please specify power cord and language options when ordering.

Recommended Accessories

Logic Analyzer Cart – LACART, K4000.

TLA5000 Rackmount Kit – Order 016-1887-00.

TLA5000 Wheeled Transport Case – Order 016-1937-00.

TLA7QS – TLA Family training package. (TLA configuration required: 102 channels).

TLA7QS Technical Reference Support Kit – Order 020-2211-02.

TLA7QS Quickstart Training Manual – Order 070-9717-05.

TLA5000 Service Manual– Order 071-1305-00.

TLACAL1– TLA520x Performance Verification and Adjustment Fixture.

Options

Instrument options

Opt. 1C – Add iView external oscilloscope cable kit (012-1614-02).

Opt. 1P – Add full complement of P6418 17-Channel general-purpose probes (each includes two 8-Channel leadsets, one 1-Channel leadset, 20 SMT KlipChip™ grabber tips).

Opt. 2P – Add full complement of P6434 34-Channel high-density Mictor probes.

Opt. 3P – Add full complement of P6417 17-Channel general-purpose probes that allow you to separate the 8-Channel podlet groups into channels (each includes two 8-Channel leadsets, one 1-Channel leadset, 20 SMT KlipChip grabber tips).

Opt. 4P – Add full complement of P6419 17-Channel high-density compression probes.

Option	TLA5201	TLA5202	TLA5203	TLA5204
1P Add P6418 Probes	2	4	6	8
2P Add P6434 Probes	1	2	3	4
3P Add P6417 Probes	2	4	6	8
4P Add P6419 Probes	2	4	6	8

Opt. 7S – Increase to 2 Mb base memory depth per channel.

Opt. 8S – Increase to 8 Mb base memory depth per channel.

Service Options

Opt. C3 – Calibration Service 3 Years.

Opt. C5 – Calibration Service 5 Years.

Opt. D1 – Calibration Data Report.

Opt. D3 – Calibration Data Report 3 Years (with Option C3).

Opt. D5 – Calibration Data Report 5 Years (with Option C5).

Opt. R3 – Repair Service 3 Years.

Opt. R5 – Repair Service 5 Years.

International Power Plugs

A0 – North America power.

A1 – Universal EURO power.

A2 – United Kingdom power.

A3 – Australia power.

A4 – 240 V, North America power.

A5 – Switzerland power.

A6 – Japan power.

A10 – China power.

A99 – No power cord or AC adapter.

Software

TLA5000 Series Product Software CD – Order 063-3487-02.

TLA5000 Series Operating System Restore CD – Order 063-3672-00.

Language Options

Opt. L0 – English Manuals.

Opt. L10 – Russian Manuals.

Opt. L99 – No Manuals.

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Our most up-to-date product information is available at:
www.tektronix.com

Product(s) are manufactured in ISO registered facilities.

Product(s) complies with IEEE Standard 488.1-1987, RS-232-C, and with Tektronix Standard Codes and Formats.

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